



JC10 Rec'd PCT/50 02 NOV 2005

ASA-1236

PCT  
#15

UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Komiya, et al  
Serial No.: 10/533,127  
Filed: April 29, 2005  
For: DEFECT ANALYSIS APPARATUS, SYSTEM AND METHOD FOR  
SEMICONDUCTOR INTEGRATED CIRCUIT

**INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR 1.97 & 1.98**

November 2, 2005

Mail Stop Amendments  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In the matter of the above-identified application, applicants are submitting herewith a copy of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted before the mailing date of a first office action on the merits.

Although one of the documents listed on the attached form equivalent to Form PTO-1449 is not in the English language, the requirement of 37 CFR 1.98 (a) (3) for a concise explanation of the relevance is satisfied by the attached English language abstract.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Mattingly, Stanger, Malur & Brundidge, P.C. Deposit Account No. 50-1417 (Case:ASA-1236), and please credit any excess fees to such deposit account.

Respectfully submitted,

Mattingly, Stanger, Malur & Brundidge, P.C.

  
\_\_\_\_\_  
Carl X. Brundidge  
Registration No. 29,621

CIB/nac

Attachments



Form PTO-1449	DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. ASA-1236	SERIAL NO. 10/533,127
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use several sheets if necessary)		APPLICANT Yasumaro KOMIYA, et al	
		FILING DATE November 2, 2005	GROUP Not Yet Assigned

**U.S. PATENT DOCUMENTS**

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
AA						
AB						
AC						
AD						
AE						
AF						
AG						
AH						
AI						
AJ						
AK						
AL						

**FOREIGN PATENT DOCUMENTS**

Examiner Initial	Document Number	Date	Country	Class	Subclass	Abstract	
						Yes	No
AM	2001-166012	06/01	JP			x	
AN							
AO							
AP							
AQ							
AR							
AS							
AT							

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

AU	CMOS Open Defect Detection by Supply Current Test, by Masaki HASHIZUME, et al., Proc. of IEEE International Workshop on Defect Based Testing, pp. 509-513, publ. March. 2001.
AV	
AW	
AX	
AY	
AZ	
Examiner	
Date Considered	